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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,529	09/26/2003	Norihisa Arai	240800US-2S DIV	6513
22850	7590	10/05/2004	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			ROSE, KIESHA L	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/670,529

**Applicant(s)**

ARAI, NORIHISA

**Examiner**

Kiesha L. Rose

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☐ Claim(s) \_\_\_\_ is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 18-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 9/26/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

### **DETAILED ACTION**

This Office Action is in response to the filing of the application.

#### ***Drawings***

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

Fig. 12D #115

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 18-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant's Prior Art (Fig. 12d).

Applicant's Prior Art discloses a semiconductor device (Fig. 12d) that contains a semiconductor substrate (101), a first conductivity type transistor forming area (103) and a second conductivity type transistor forming area (102), a gate oxide film (108) formed on an element forming region of the substrate doped with boron or phosphorus, a shallow trench insulation film (110) formed in an element isolation region of the substrate, a channel region (105/107) formed in the first and second conductive type transistor forming area of the element forming region beneath the gate oxide and being doped with boron or phosphorus, a gate electrode film formed on the gate oxide film including a first conductive film (floating gate) (109) formed on the gate oxide doped with boron or phosphorus and a second conductive film (111) formed on the first conductive film, wherein the shallow trench insulation film has an upper surface positioned at a height between an upper surface and lower surface of the gate electrode film.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Moriyama (JP 06268178).

Applicant's Prior Art discloses all the limitations except for the gate insulation and first conductive film have an impurity concentration peak in the substrate. Whereas Moriyama discloses a semiconductor device (Fig. 4) that contains a gate oxide (12) over the substrate (11), a gate (14) formed over gate oxide where impurities are implanted to for a concentration peak in the substrate. The concentration peaks in the substrate are formed to control threshold voltage. (Purpose) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of the Applicant's Prior Art by incorporating the gate insulation and first conductive film to have an impurity concentration peak in the substrate to control threshold voltage as taught by Moriyama.

Claims 24-27 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Fig. 12d) in view of Lin (U.S. Patent 6,297,082).

Applicant's Prior Art discloses a semiconductor device (Fig. 12d) that contains a semiconductor substrate (101), a first conductivity type transistor forming area (103) and a second conductivity type transistor forming area (102), a gate oxide film (108)

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formed on an element forming region of the substrate doped with boron or phosphorus, a shallow trench insulation film (110) formed in an element isolation region of the substrate, a channel region (105/107) formed in the first and second conductive type transistor forming area of the element forming region beneath the gate oxide and being doped with boron or phosphorus, a gate electrode film formed on the gate oxide film including a first conductive film (floating gate) (109) formed on the gate oxide doped with boron or phosphorus and a second conductive film (111) formed on the first conductive film, wherein the shallow trench insulation film has an upper surface positioned at a height between an upper surface and lower surface of the gate electrode film. Applicant's Prior Art discloses all the limitations except for first and second gate insulation films with the first having a thickness larger than the second gate insulation film. Whereas Lin discloses a semiconductor device (Fig. 2f) that contains a substrate (200) with a first gate oxide (204b) and a second gate oxide (204a) where the first gate oxide has a thickness larger than the second gate oxide and has a breakdown voltage higher than the second gate oxide. The first gate oxide has a thickness larger than the second gate oxide to have dual threshold voltages. (Column 3, lines 28-65) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Applicant's Prior Art by incorporating a first and second gate oxide where the first gate oxide has a thickness larger than the second to have dual threshold voltages as taught by Lin.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art and Lin in view of Moriyama (JP 06268178).

Applicant's Prior Art discloses all the limitations except for the gate insulation and first conductive film have an impurity concentration peak in the substrate. Whereas Moriyama discloses a semiconductor device (Fig. 4) that contains a gate oxide (12) over the substrate (11), a gate (14) formed over gate oxide where impurities are implanted to form a concentration peak in the substrate. The concentration peaks in the substrate are formed to control threshold voltage. (Purpose) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of the Applicant's Prior Art by incorporating the gate insulation and first conductive film to have an impurity concentration peak in the substrate to control threshold voltage as taught by Moriyama.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art and Lin in view of Shida (U.S. Patent 6,049,113).

Applicant's Prior Art and Lin disclose all the limitations except for the first and second transistor areas have different threshold values. Whereas Shida discloses a semiconductor device (Fig. 1) that contains a first and second transistor forming area, where the first and second transistor forming areas have different threshold voltages. The first and second transistor forming areas have different threshold voltages to prevent punchthrough. (Column 6, lines 25-67 and Column 7, lines 1-27) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Applicant's Prior Art and Lin by incorporating the first and second transistor forming areas to have different threshold voltages to prevent punchthrough as taught by Shida.

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
KLR

  
AMIR ZARABIAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800